

# **Virtual Prototyping**

## **Digital Signal Processing Systems**

**September 23, 1998**

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Moorestown, NJ**

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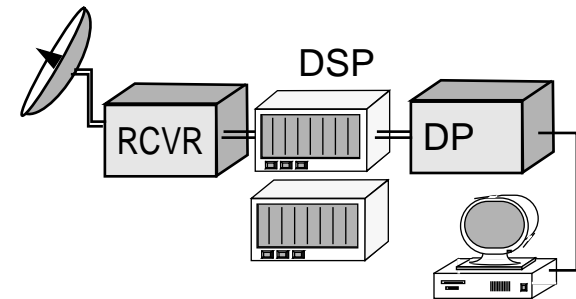
**Lockheed Martin  
Advanced Technology Laboratories  
A&E Bldg.-2W, Camden NJ 08102**

## Radar DSP Virtual Prototyping

- **Virtual Prototyping addresses complex risks early:**
  - Improves design quality & reduces design cycle.
  - Involves many challenges.
- **ATL has applied effective prototyping techniques on recent projects:**
  - Synthetic Aperture Radar (SAR) Signal Processor
  - STAP AEW
  - Echo Track Classifier
  - TBMD-EDM
  - SAR Semi-Automated IMINT Processor (SAIP)
  - Radar Signal Processor (>60 chassis !)
- **Hardware complexity prototyped ranged from 16 to 1000+ processors.**
- **Software applications contained up to 11,000 tasks.**
- **Prototyped at multiple distinct abstraction levels:**
  - Algorithmic, Performance, Behavioral.
- **Virtual prototyping was central to SAIP project:**
  - Reduced processing system volume by 100:1.

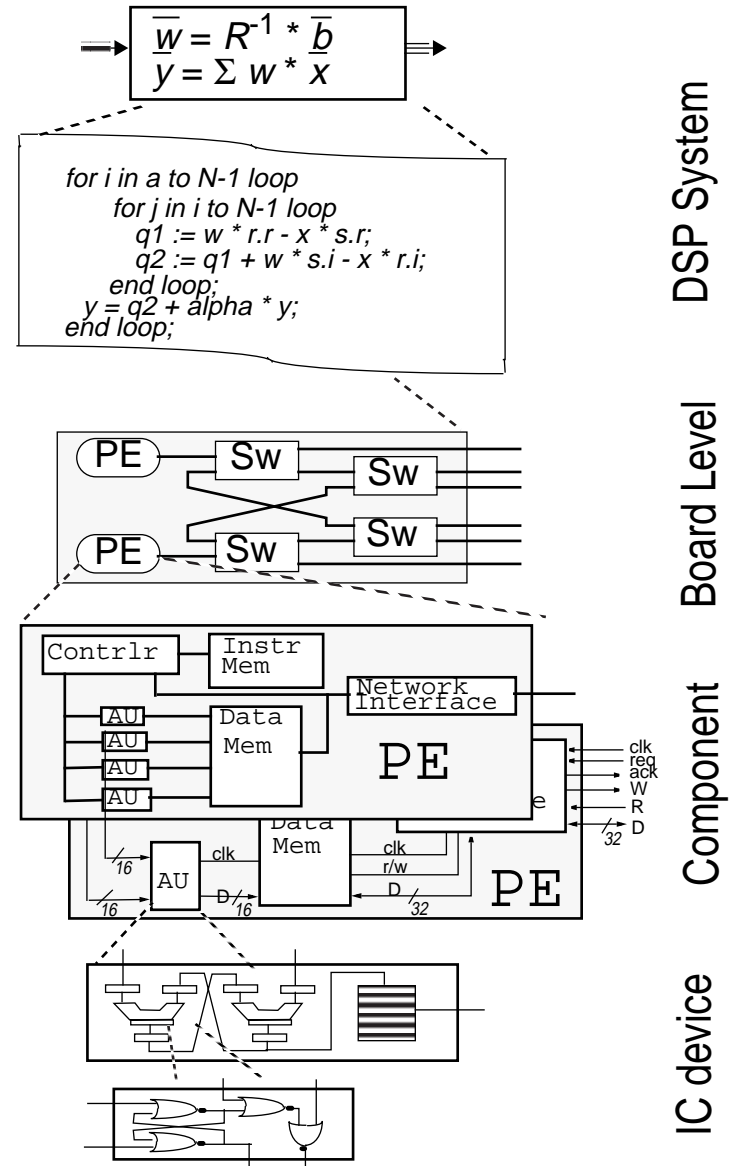
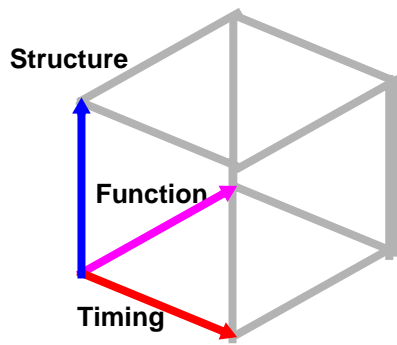
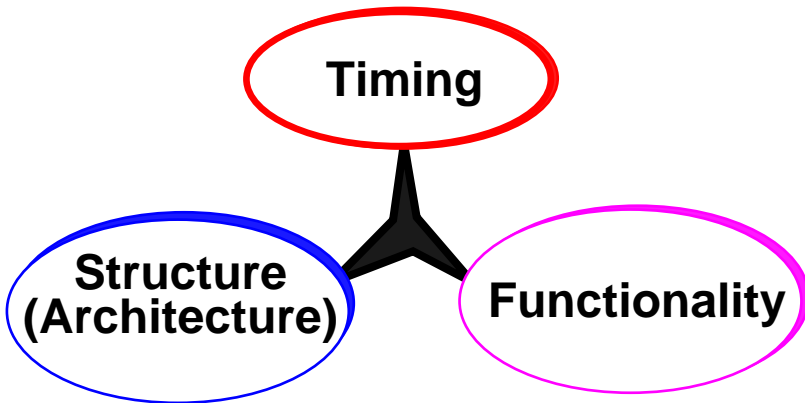
## Background

- Radar signal processing unique application challenges:
  - High data rates, arithmetically intensive, real-time low-latency processing.
  - More resolution, more sophisticated algorithms.
  - Move analog functions to digital domain.
  - Trade system budgets for cost effective DSP processing.
  - Increased emphasis on COTS  $\mu$ Procs.
  - Minimize size, weight, power.
  - Efficiently use complex resources
- High degree of parallelism – Difficult software design problem.
  - Architecture evaluation/selection.
  - Network bottlenecks, latency, throughput.
  - Software to hardware mapping,
  - Data storage/transfers,
  - Schedule computations / data-moves
  - Establish low-level requirements
- Virtual Prototype
  - Computer-based model or software-based simulation.
  - Purpose: testing, exploration, demonstration, validation, design aid.
  - Can be abstract. Addresses only the issues at hand.
  - Design changes can be done in minutes.



# Virtual Prototyping Concepts

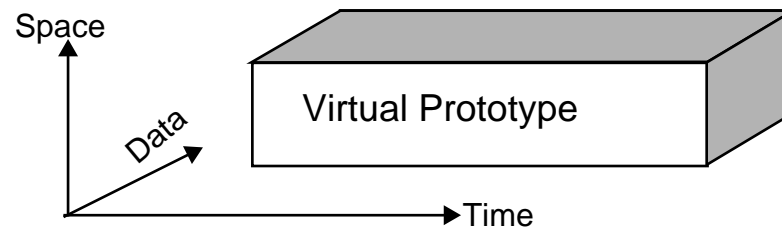
- Describe:  
Structure, Function, Concurrency
- Multiple Abstraction Levels:



## Virtual Prototype Focus:

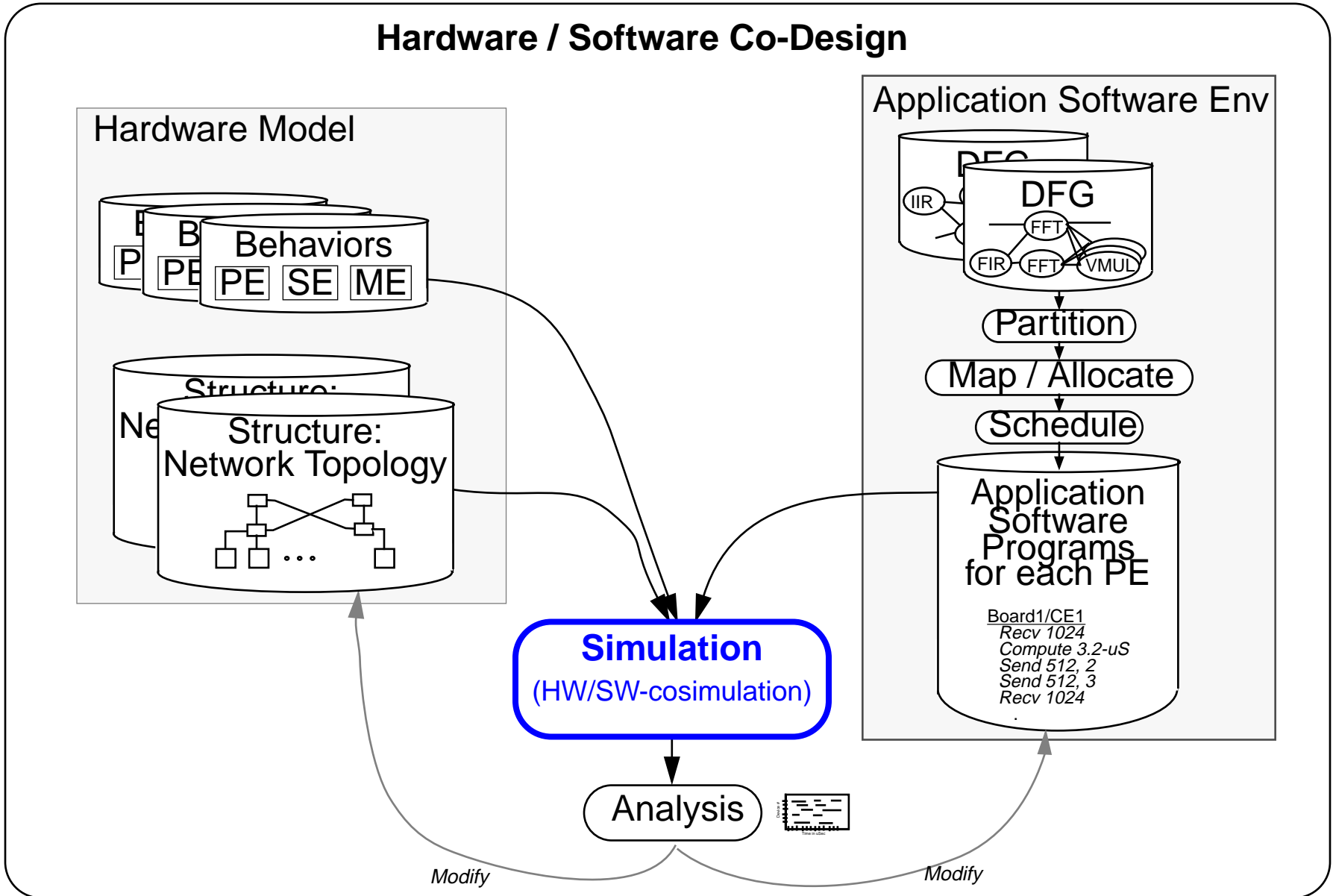
- **Facilitates:**

- System Sizing – Number and type of processors, memory sizes.
- Architecture Selection – Link bandwidths, protocols, topology configs.
- Hardware - Software mapping
  - Early integration of software with hardware
  - Application partitioning and allocation
  - Task scheduling and flow control
- Concept verification– Processor/link utilizations, throughput & latency
- Test system's interaction with related systems
- Visualize, understand, optimize, and demonstrate prior to construction.
- Powerful development aid for target system,  
Provides non-invasive observation of all data values at all times.



# System Architecture Simulation Approach

## Hardware / Software Co-Design



## Candidate Environments

- ATL uses and evaluates many candidate prototyping tools.

### Candidate Languages/Tools:

C, Java, C++

Verilog

Modsim II

Mil3 OPNET

Mathworks Simulink

Cadence BONEs

SES Workbench

ADAS

Nuthena Foresight

ATL CSIM

ObjecTime

Caci Network 2.5

Mathworks Matlab

I-Logix Statemate

UCB Ptolemy

Omniview Cosmos

Pure Analysis

- Domain specific tools/languages do not span abstraction hierarchy.
- Others are based on proprietary closed-end languages.
- C, C++, Java, Fortran - Describe function, but have no inherent notion of physical structure or time.
- Net based CAD languages - Describe structure and simple timing, but have no notion of high level function or abstract timing.
- ATL's CSIM environment adds structure and timing description capabilities to the standard C language, plus graphical tools.  
Optimized for these type of radar DSP applications from use and need.

## Virtual Prototype Examples

- Recent examples of virtual prototyped DSP systems:
  - SAR Semi-Automated IMINT Processor (SAIP), (72 processors)
  - Synthetic Aperture Radar (SAR) Signal Processor, (24 processors)
  - Echo Track Classifier (ETC), (16 processors)
  - STAP AEW, (72 processors)
  - Radar Signal Processor, (1060 Processors)
  
- Virtual Prototyping was central to the RASSP program.
  - The demonstrated capabilities were significantly advanced by RASSP.

## SAIP Virtual Prototypes

### SAIP - Semi-Automated Image-Intelligence Processor

- **Challenges:**

- 30 SAR Images per Second to be Processed

- 5-GFLOp/S Sustained Operation Rate

- 3.4-MB/S Combined Input/Output Data Rate

- Memory Requirements: HRI 7-MB, HRC 38-MB, 22.3-MB

- 100:1 Reduction in Compute Density (Computations/Volume)

- **Accomplishments:**

- Prototype of 72-processor multi-board system was configured quickly from re-usable model elements.

- Facilitated in developing optimal partitioning and mapping schemes.

- Minimized Memory Requirements

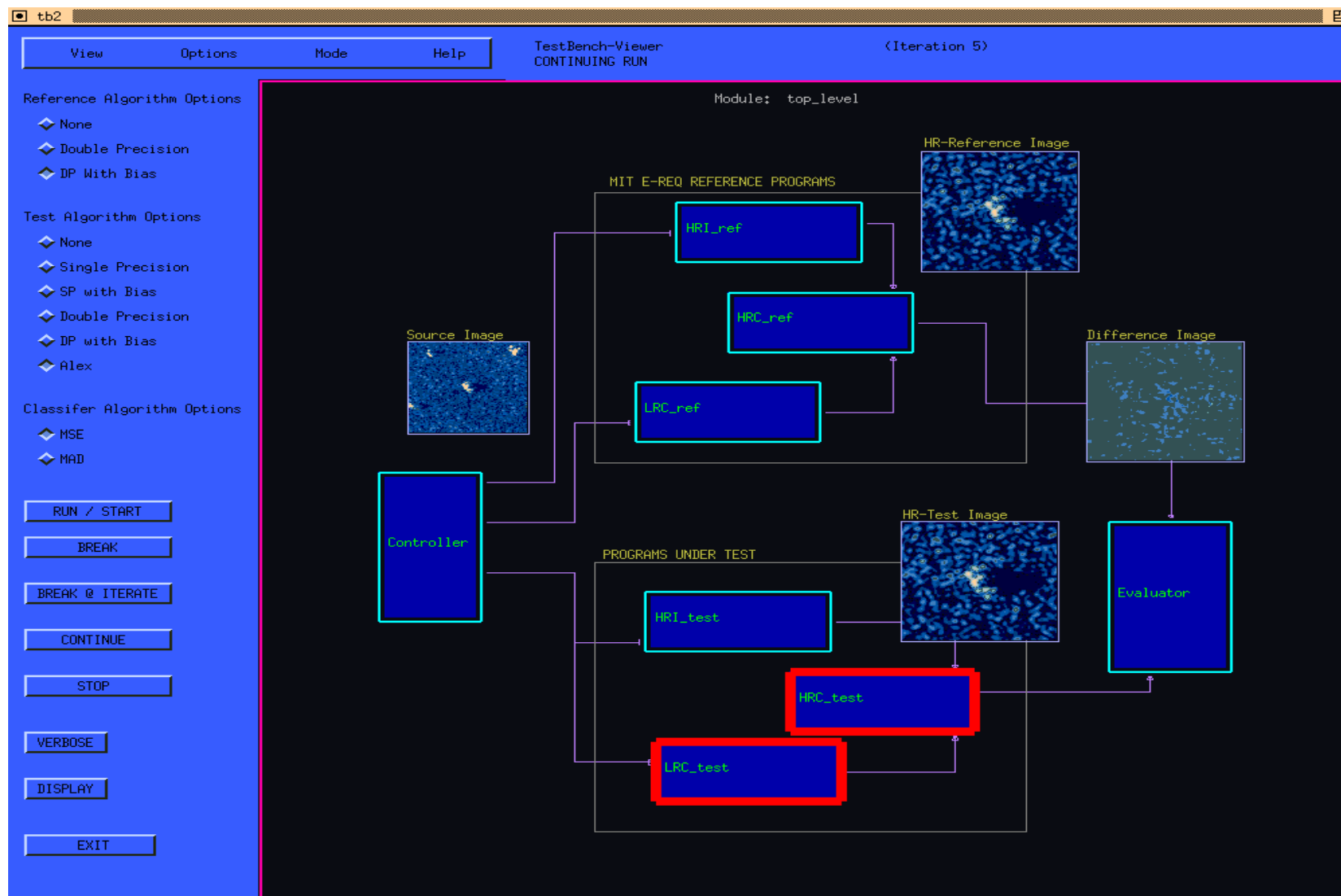
- Retired communications concerns, quantified loading/contention effects.

- Established VME bus adequacy for backplane transfers.

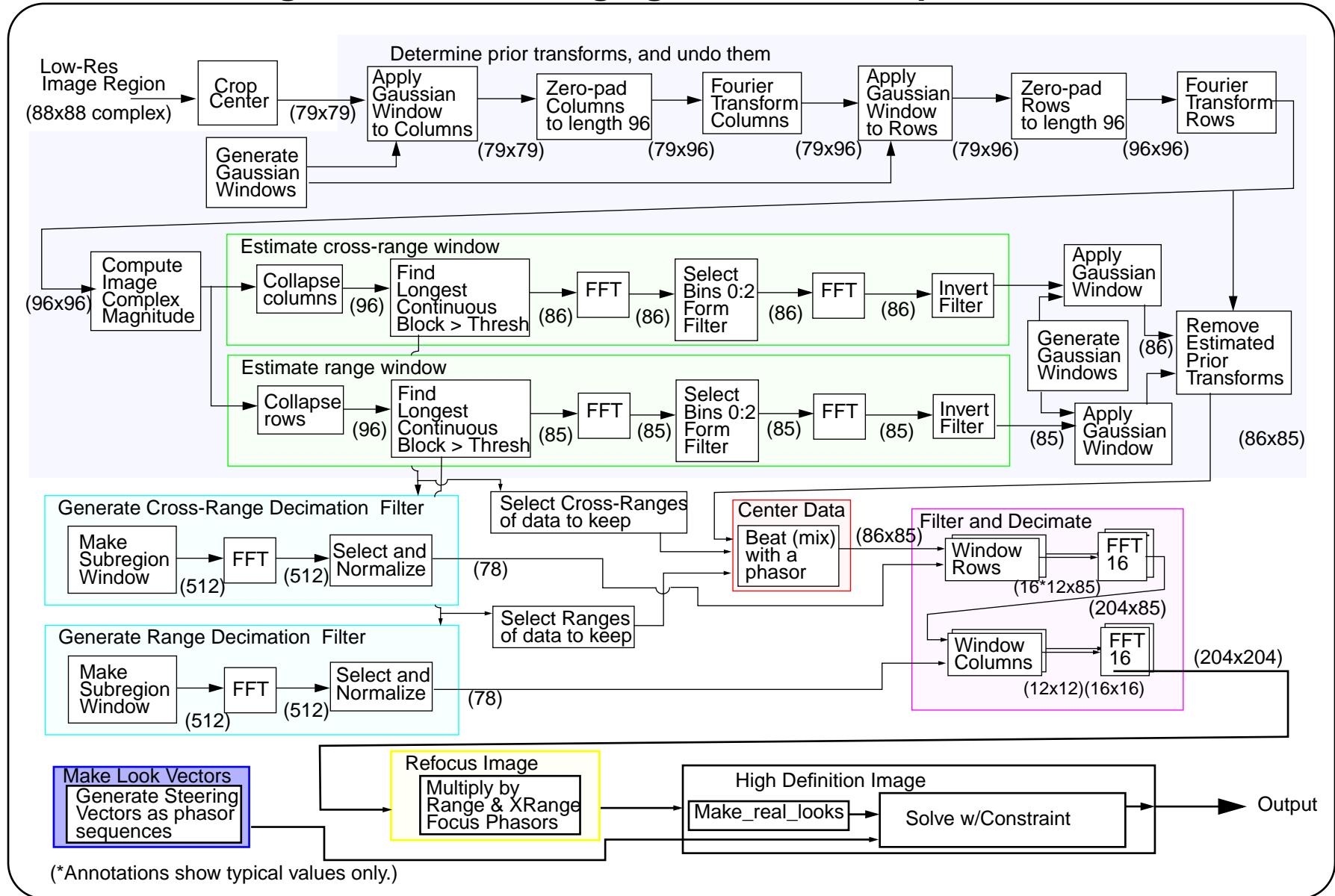
- Showed effect of random compute times on system performance.

# Algorithm Level Virtual Prototype

## Virtual Test-Bench for Algorithm Optimization

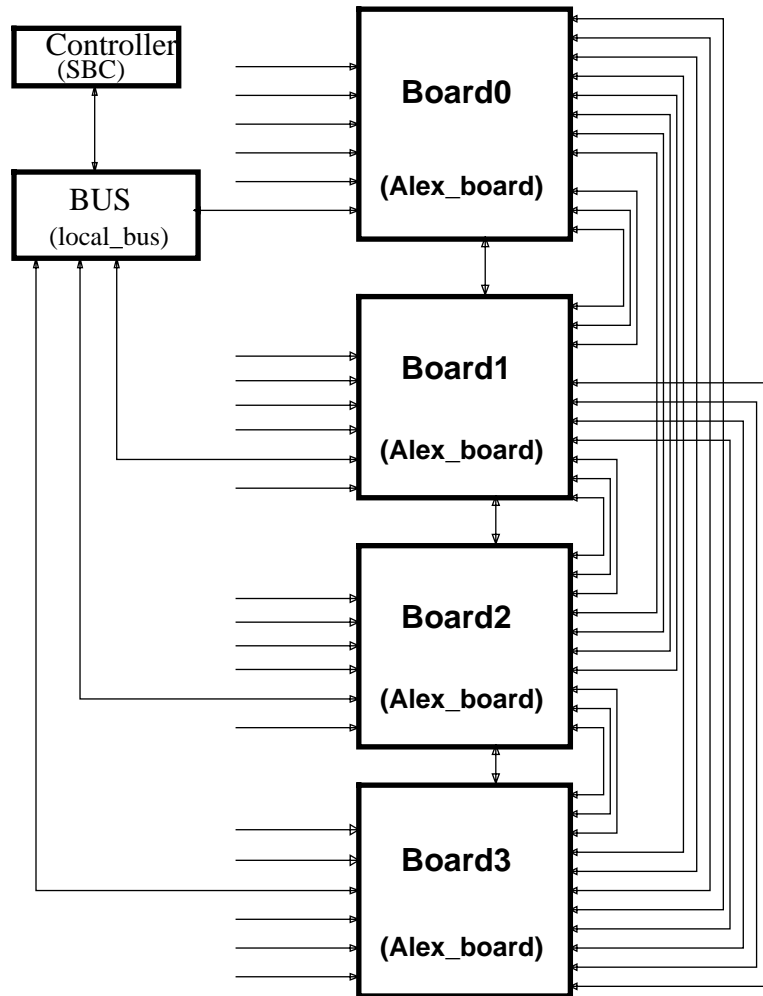


# High-Resolution Imaging Data Flow Graph

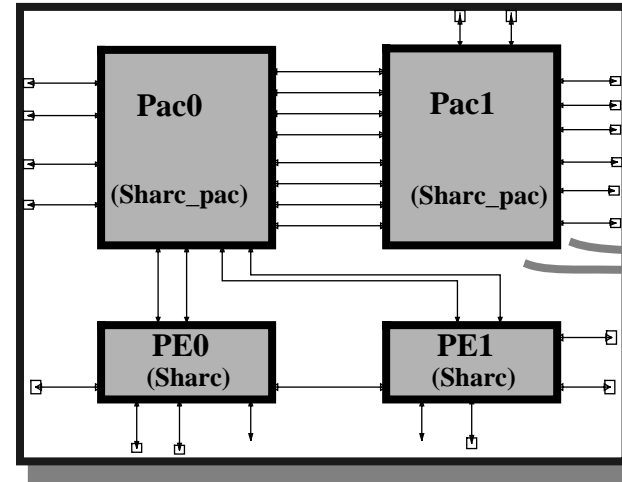


# SAIP Virtual Prototype of COTS Hardware

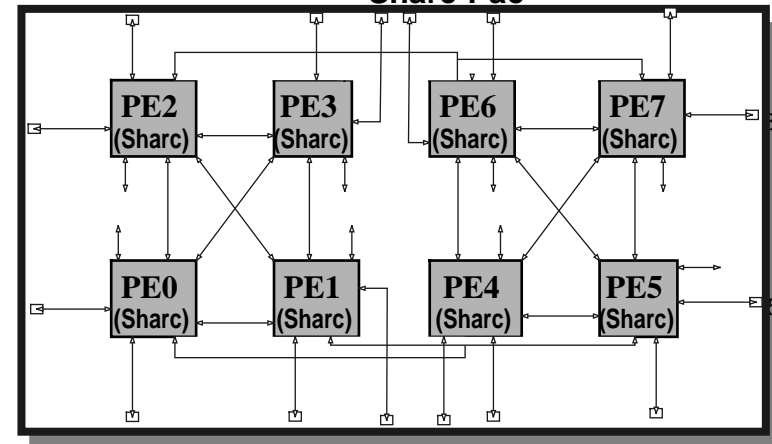
Four Board System



Alex Board



Sharc-Pac





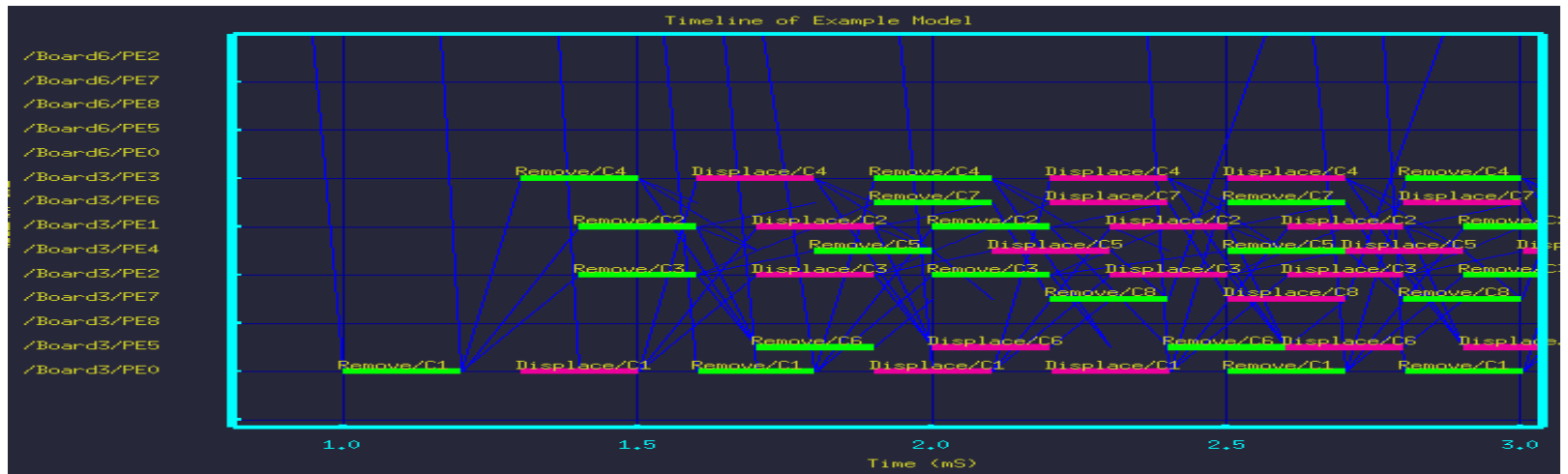
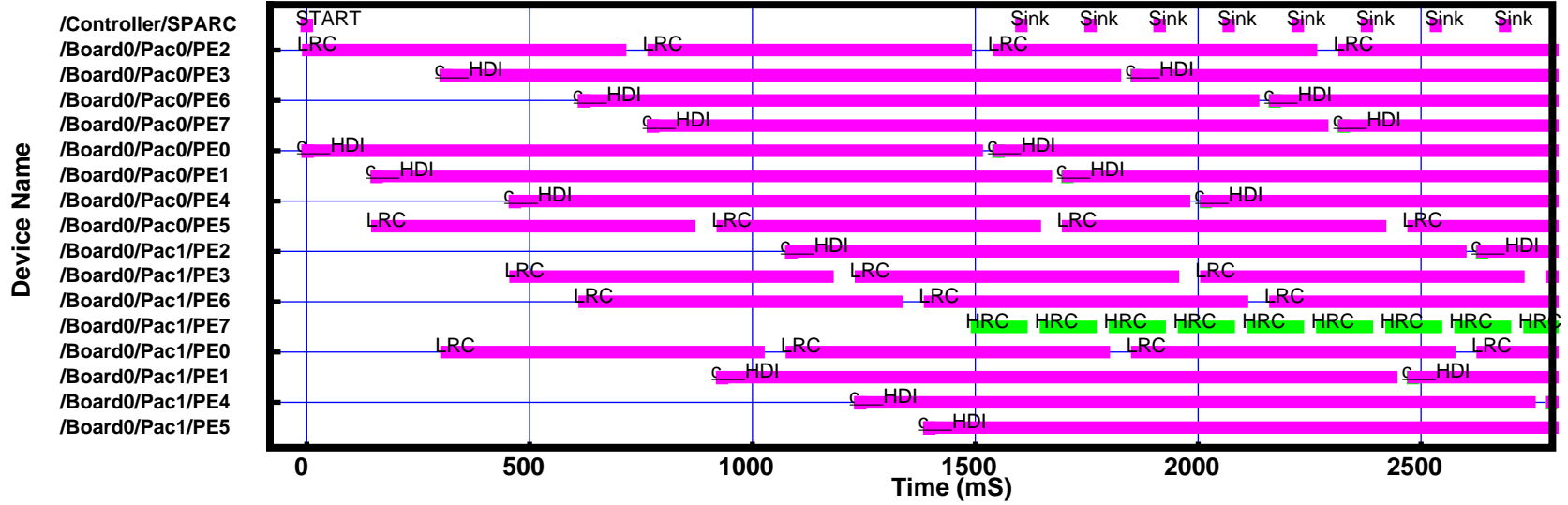
# Animating a Flattened Hierarchy

72 Processor's concurrent activities indicated by color



# SAIP Virtual Prototype Time-Line Display

## Time-Line of Hardware/Software Co-Simulation



## Virtual Prototype - (Example 2)

### Synthetic Aperture Radar (SAR) Benchmark-2

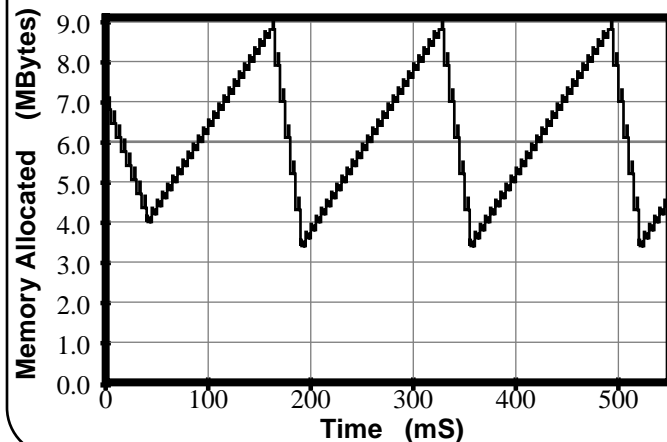
- **Challenges:**

- 27.4-MB/S input data rate
- 440-MFLOPs/Sec sustained operation rate
- < 2.0-Second Maximum Latency.
- Application flow graph contains 10,700 tasks
- Program 24 Processor Element System

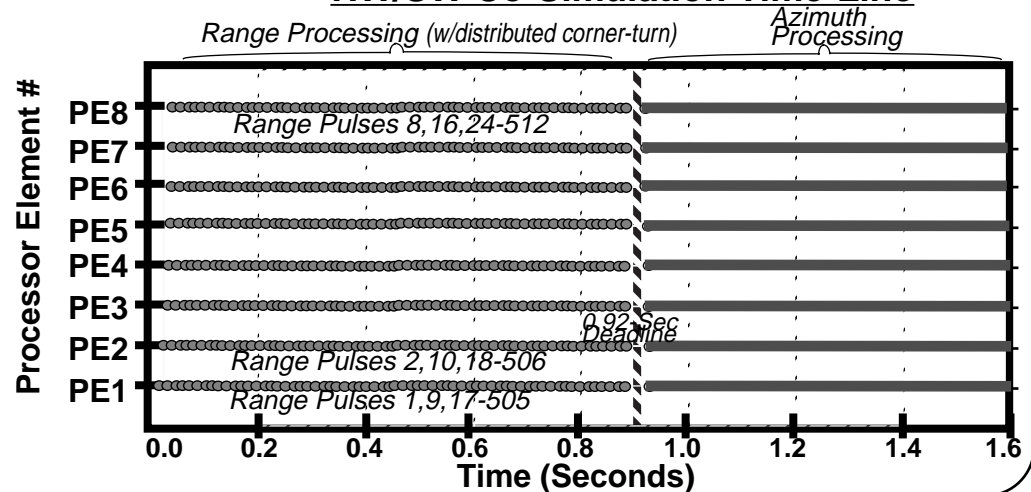
- **Accomplishments:**

- Three Levels of Virtual Prototypes Developed
- Enabled Quick Re-targeting to New Architecture
- Developed and Verified Complex Software within Two Week Period.
- Efficient Mapping Satisfied Throughput and Latency Requirements.

Memory Allocation

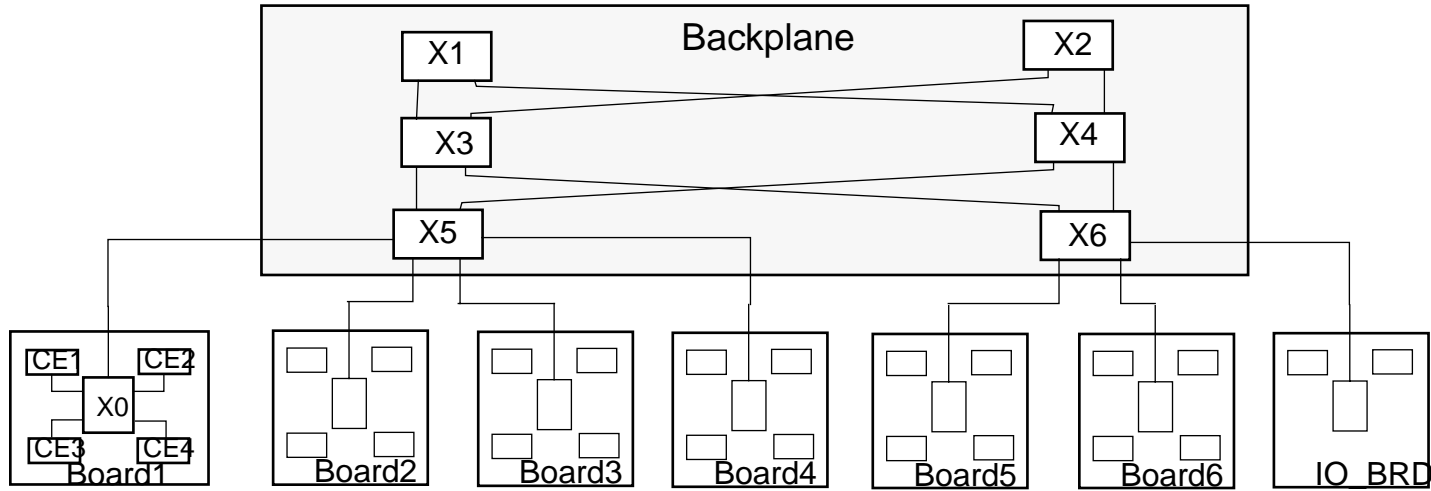


HW/SW Co-Simulation Time-Line

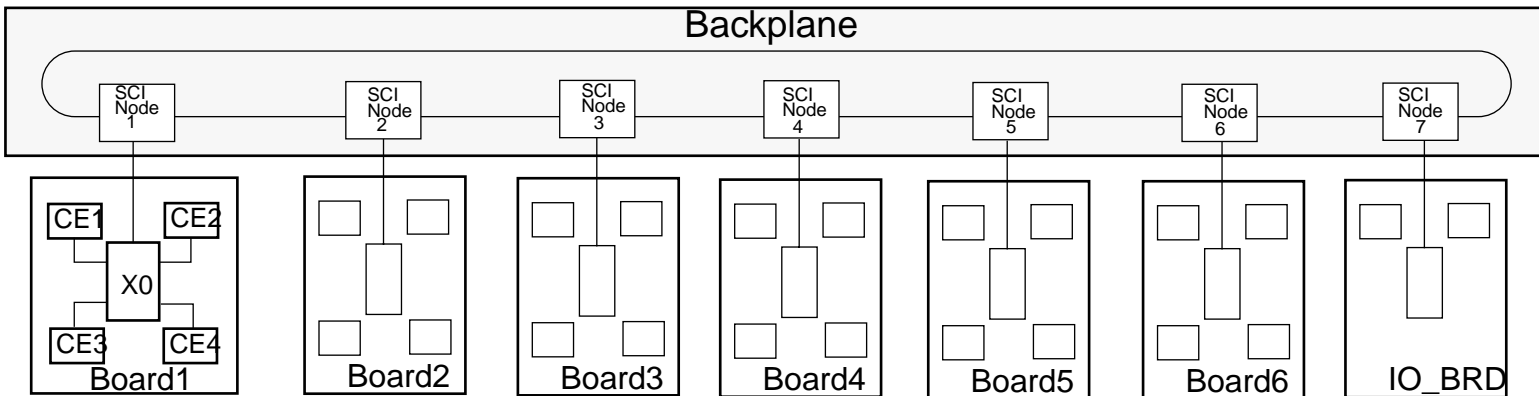


# Candidate Hardware Architectures for SAR

## Candidate Network 1 - Mercury Raceway

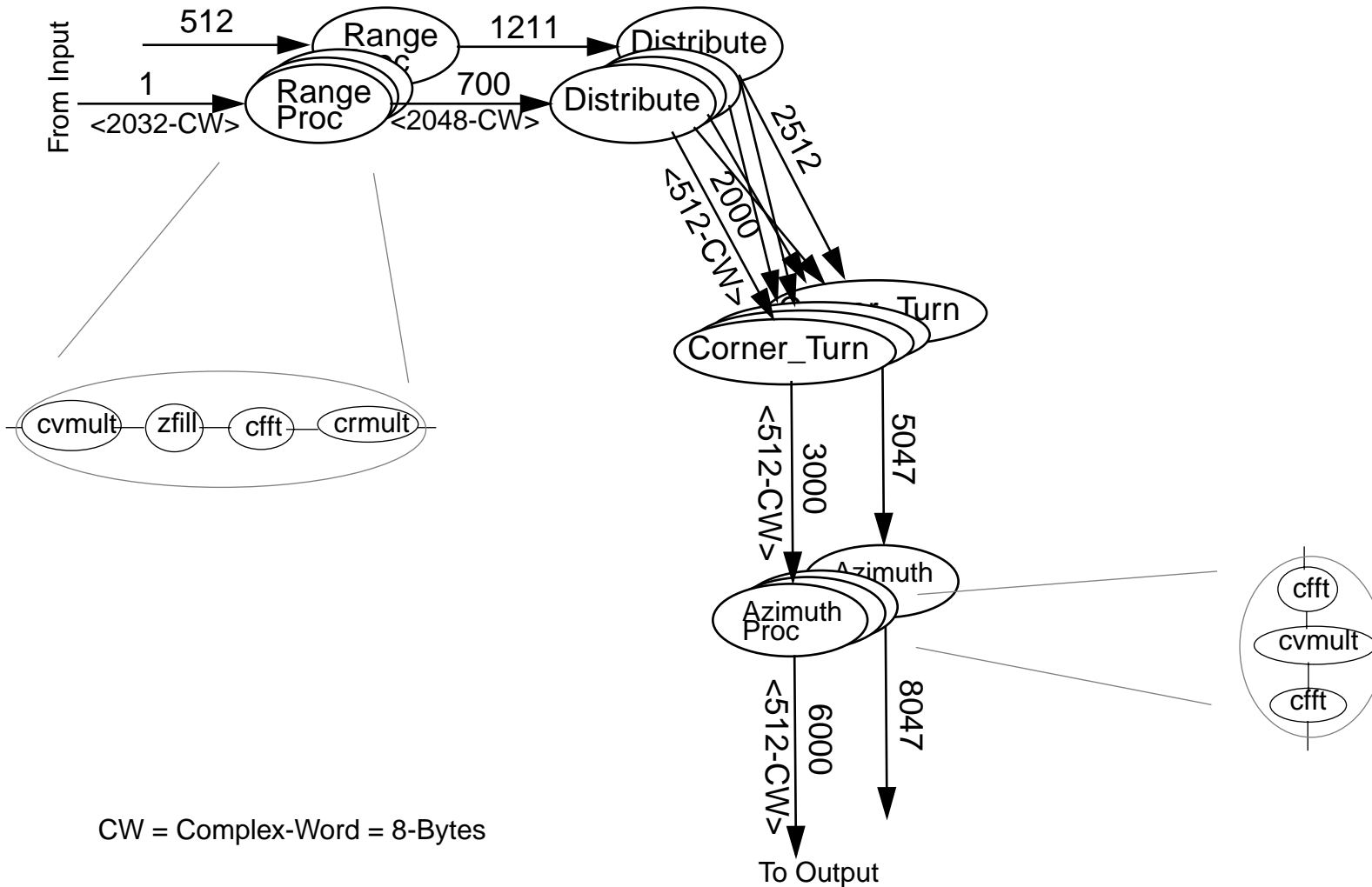


## Candidate Network 2 - Scalable Coherent Interconnect (SCI)



# SAR Software Data Flow Graph

- Synthetic Aperture Radar (SAR) Virtual Prototype DFG
- 10,752 Primitive nodes in SAR DFG, one of three polarizations



## SAR Output Image From CSIM Virtual Prototype

Four 512x2014-pixel Frames => 4-MPixels



Over 14-Million Packets  
Transferred Through  
Network

~5-Seconds of simulated  
real time processing

Produced from Virtual  
Prototype of Six (6) PE  
Networked DSP  
System.

# Virtual Prototyping

## Comparative Simulation Efficiencies

Simulation	Simulated Time	Host CPU Time	Equiv. Instructions /Sec
CSIM Perf Mod of 24-PE Sys. *	5.0-Sec	3-Mins	28,570,000
CSIM Abstr Beh of 6-PE Sys. **	5.0-Sec	7-Mins	3,081,000
VHDL ISA Model of 1 i860 PE Node *	5.0-mS	12-Hours	5

**Prototypes predicted performance to within 7% accuracy of final system.**

\*i860-XR 40-MHz, 40-MIPS

\*\* ADSP-21060 Sharc 40-MHz, 40-MIPS

## Echo Tracking Classifier (Example 3)

### Virtual Prototype - Example 3

- **Challenges:**

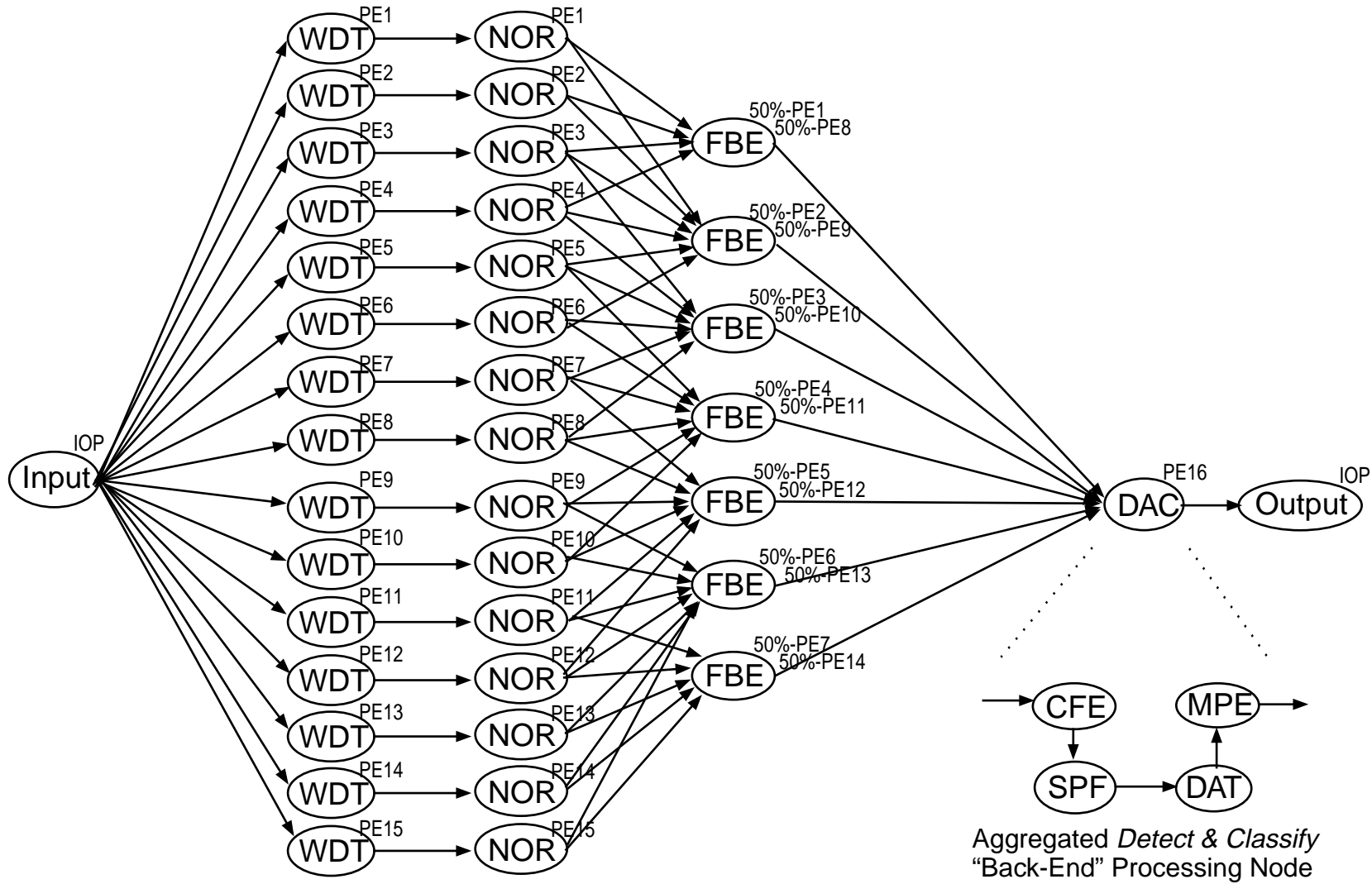
72-Beams, Update Rate = 60-Seconds, Range-samples = 32,000  
Complex algorithm decomposed into ~40 application task nodes.  
Operation rate = 23.368-MFLOPs/Sec

- **Accomplishments:**

- Prototype was configured and exercised from re-usable model elements in under 2-weeks.
- The Myrinet/Sharc-ADSP21060 FPCAP architecture was shown to satisfy baseline requirements for two applications: ETC and SAR.
- Potential software mapping strategies were developed.
- Concerns about network performance implications on system throughput were retired.
- VP brought awareness of Myrinet configuration deadlock issues.
- Local memory bus utilization was identified as architecture hotspot.

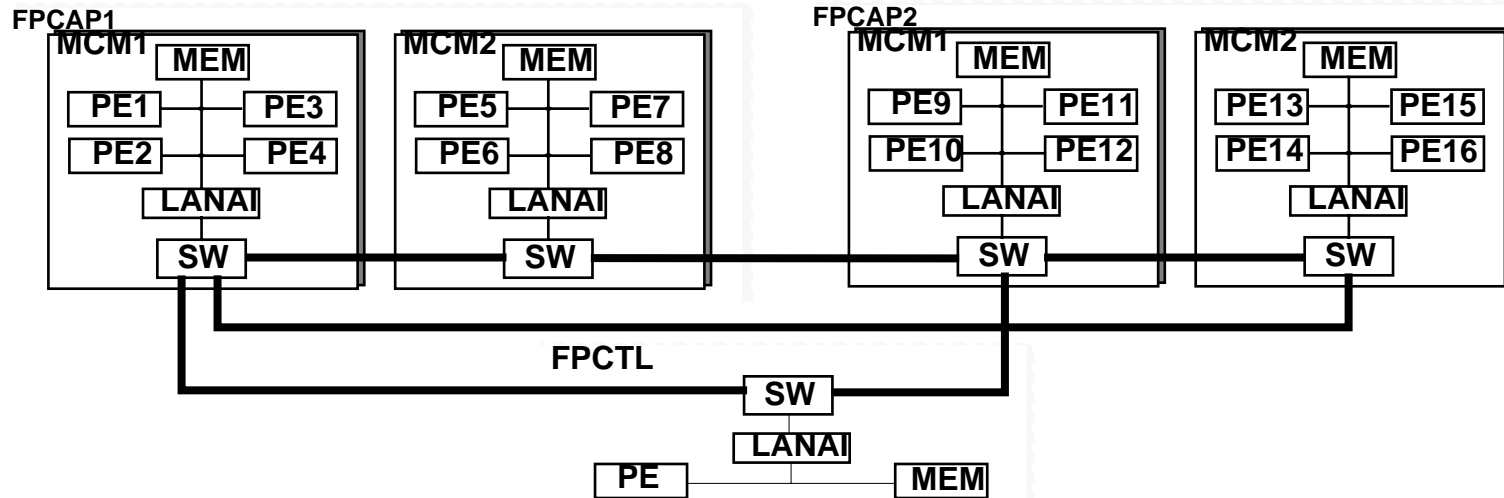
# ETC Software Data Flow Graph

## Partitioned / Aggregated Data Flow Graph (DFG) with Static Processor Element Assignments

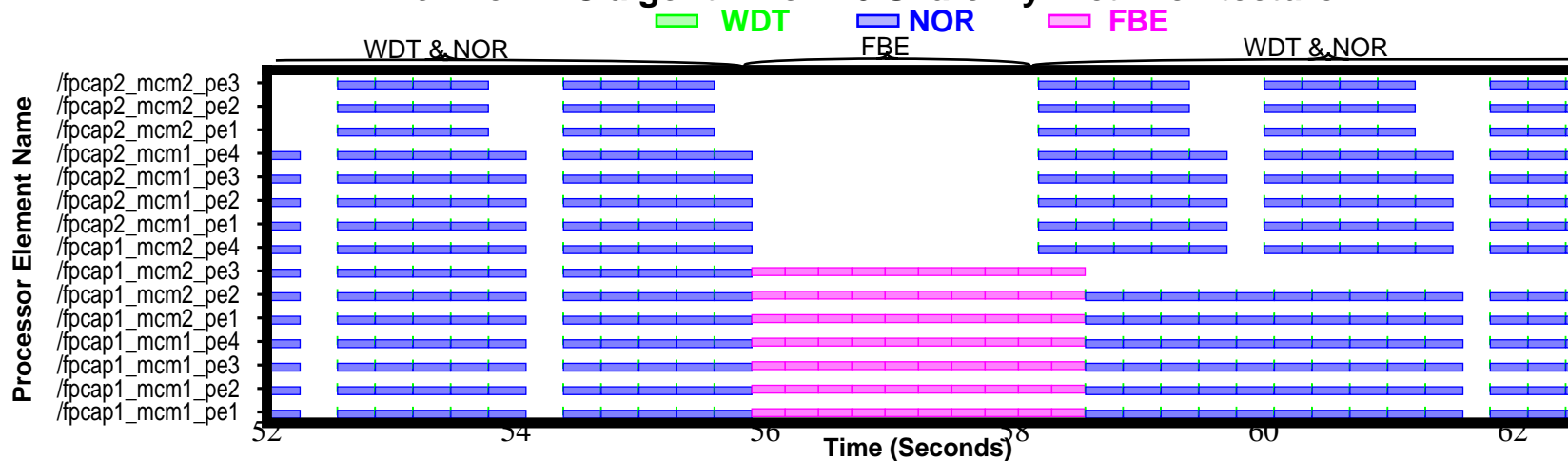


# ETC Hardware Virtual Prototype and Results

## Myrinet Network Hardware Architecture



## Time-line: ETC algorithm on 16-Sharc Myrinet Architecture



## HPSC STAP Myrinet Based RMGS System (Example 4)

### Virtual Prototype - Space-Time Adaptive Processor

- **Challenges:**

- System order > 50

- Weight Vectors to solve = 3

- ~1,600 Application Task Nodes

- Operation Rate > 1 GFLOP/S

- Throughput: > 40 KHz input rate, ~300 Hz output rate

- Latency: < 15-mS

- **Accomplishments:**

- Simulated 72 Sharc Processor system, 8-boards interconnected through Myrinet.

- Prototype was configured quickly from re-usable model elements.

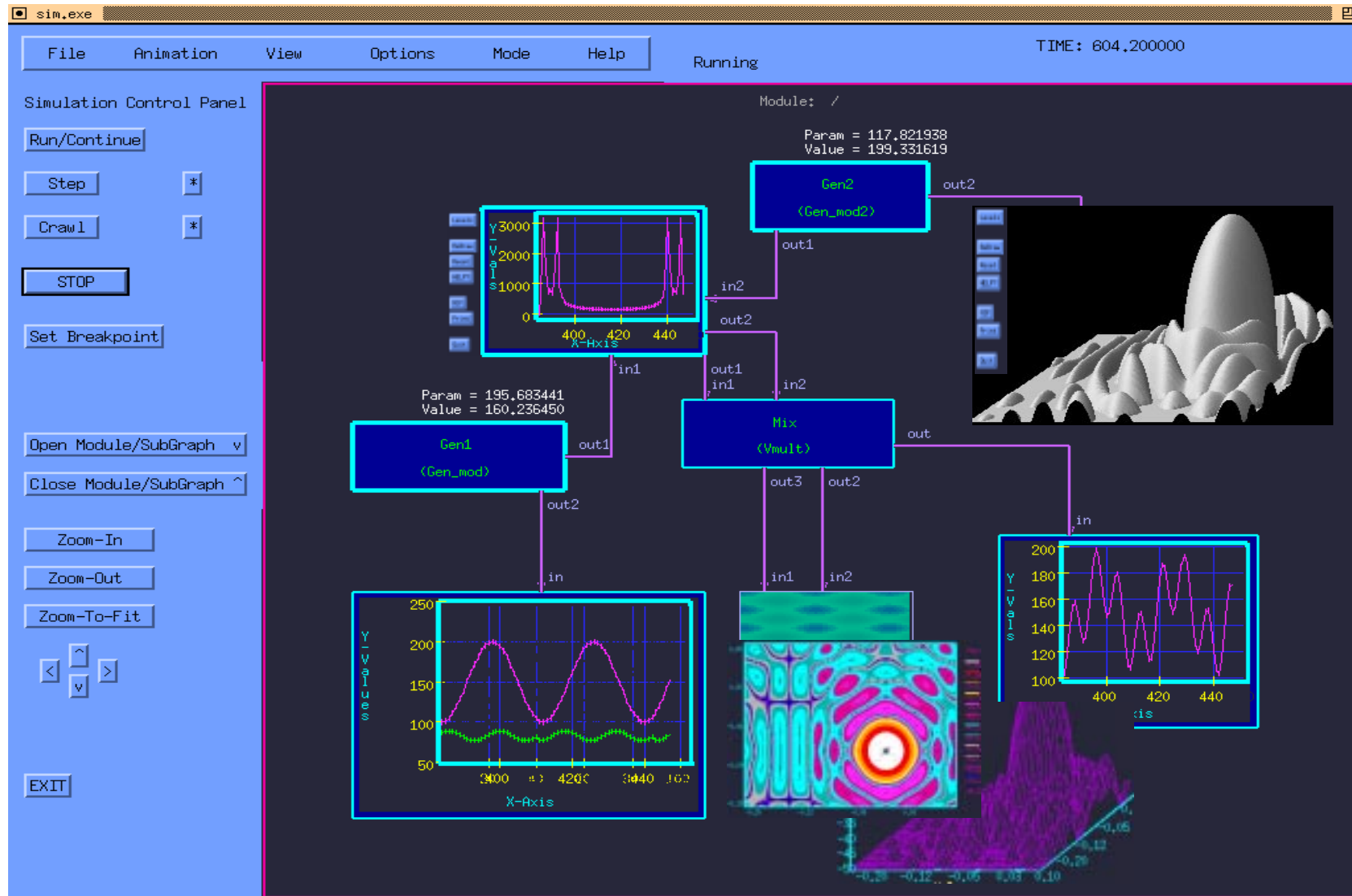
- Revealed communication transfer issues early, took corrective actions.

- Tested, Studied, and Developed three mapping approaches.

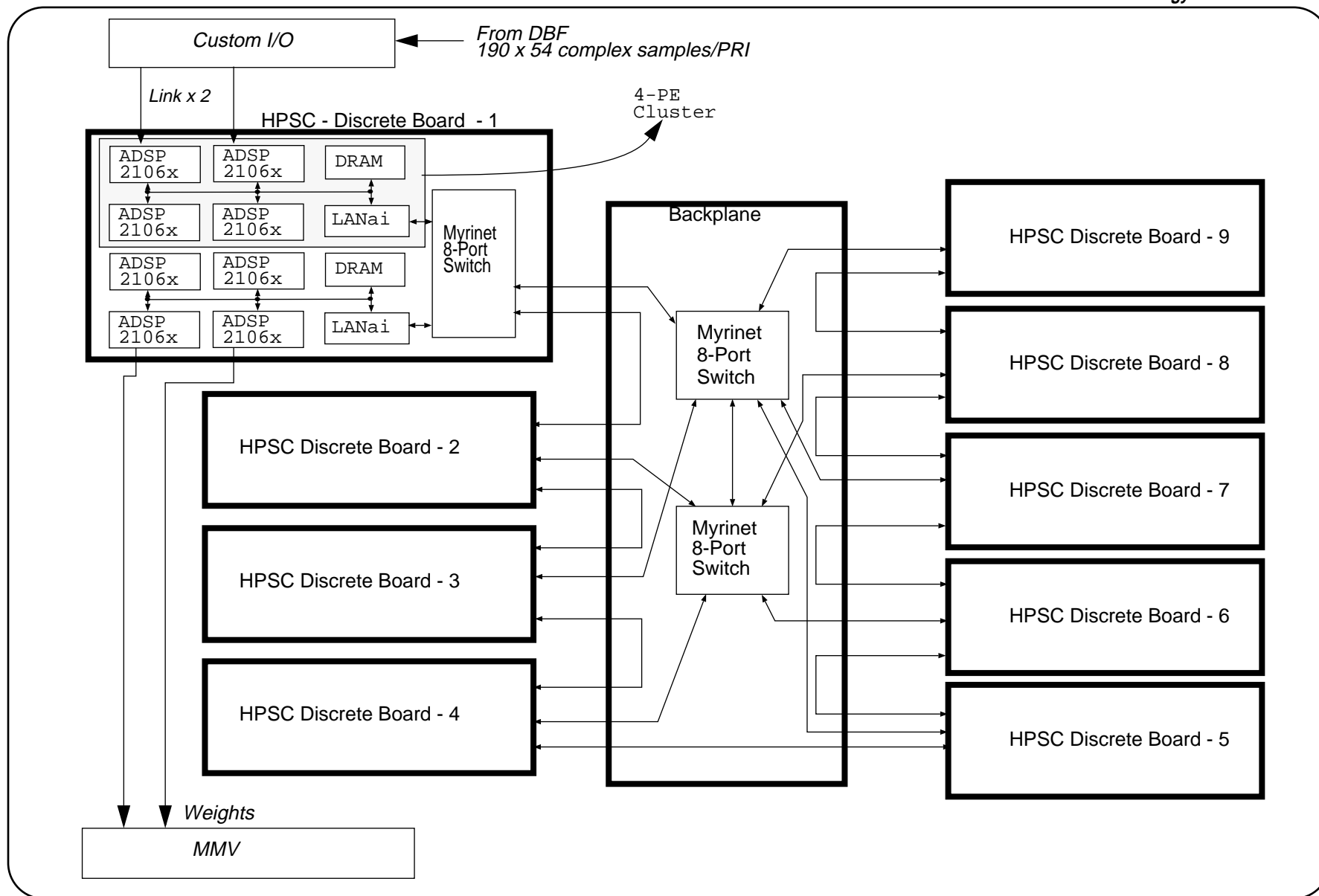
- Effects of fine grain and coarse grain mappings quantified.

- Targeted improvements to communication routines.

# Pure Algorithmic Virtual Prototype

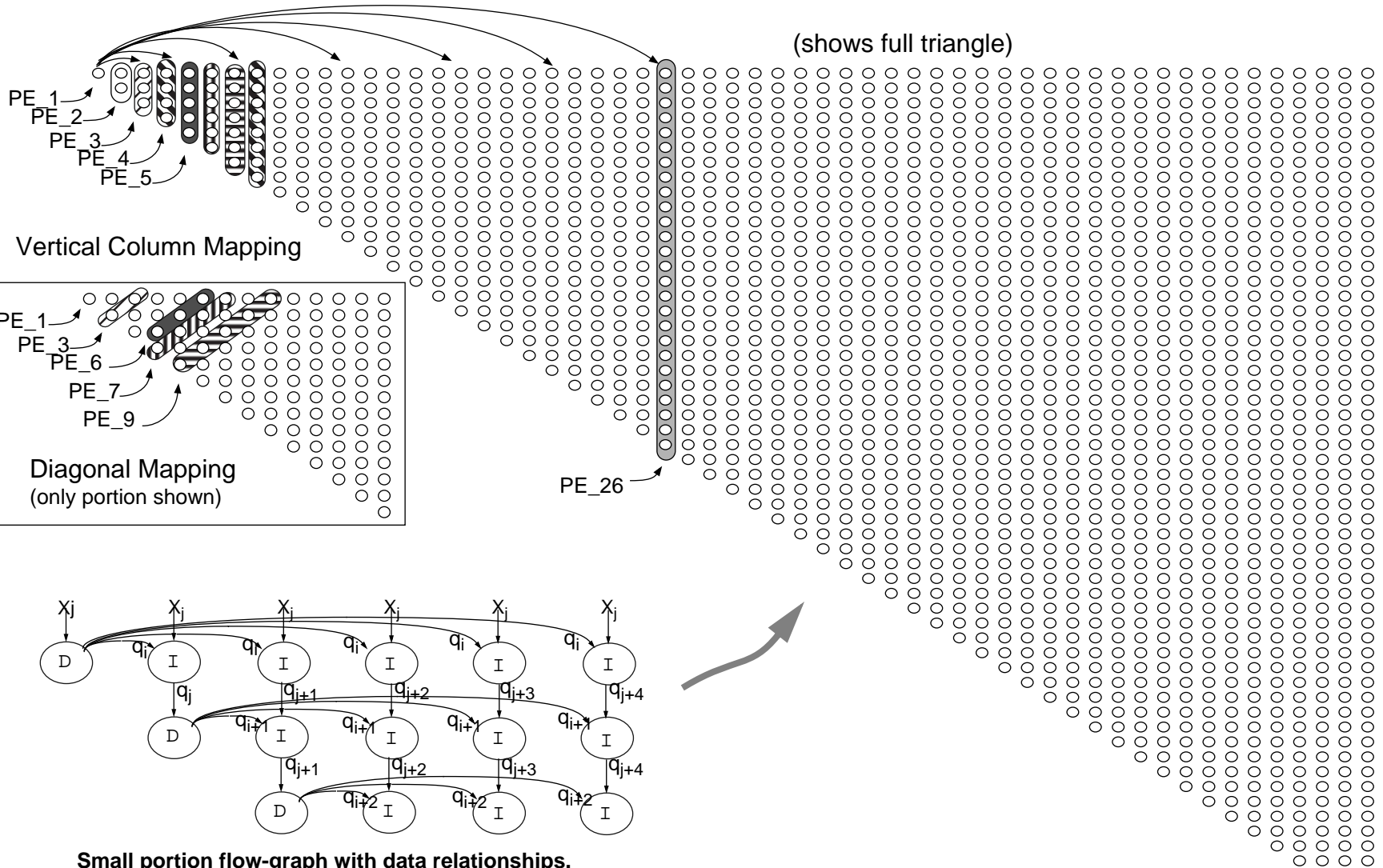


# STAP Candidate Hardware Architecture

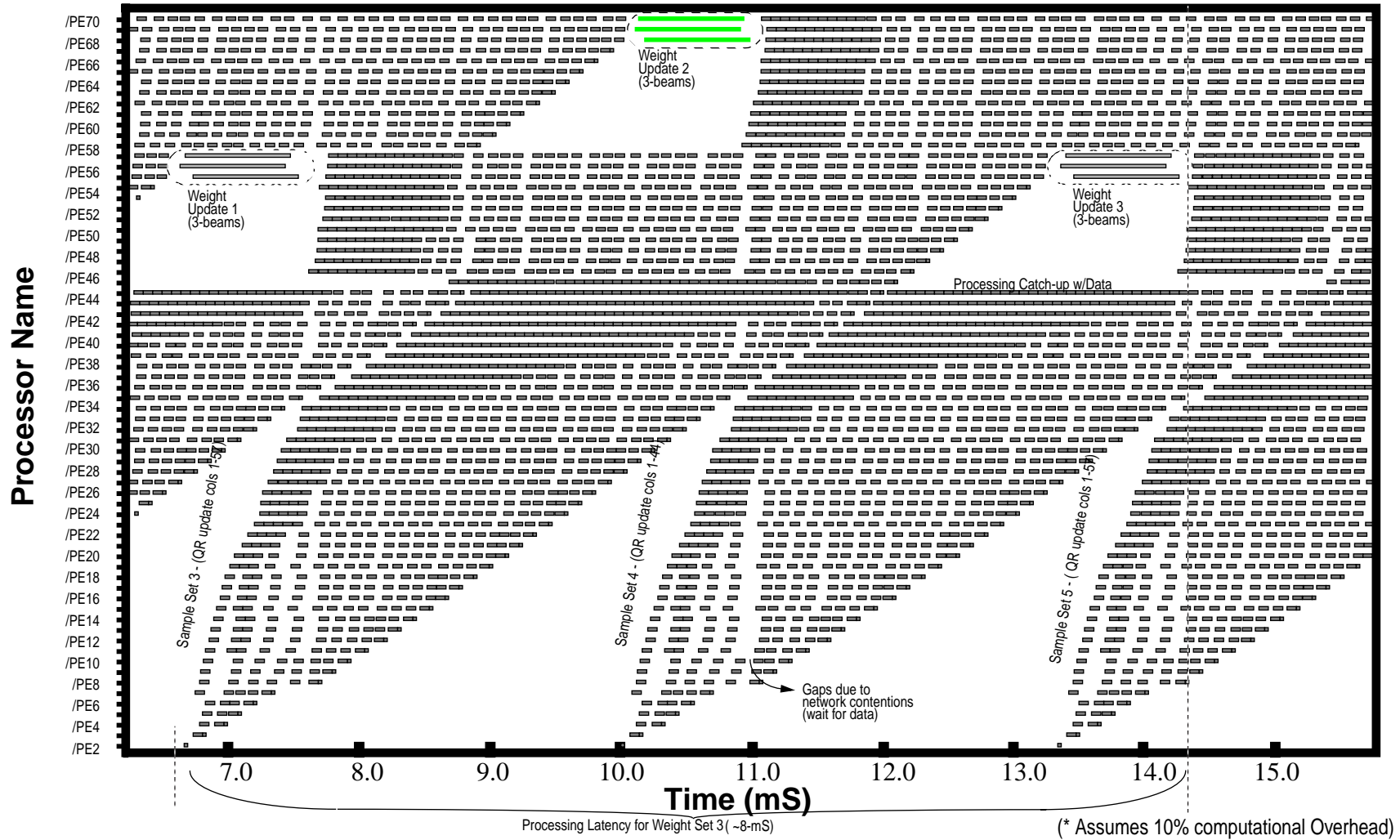


# STAP Software Data Flow Graph

## PE Mappings to Matrix Triangle for Block-Recursive RMGS

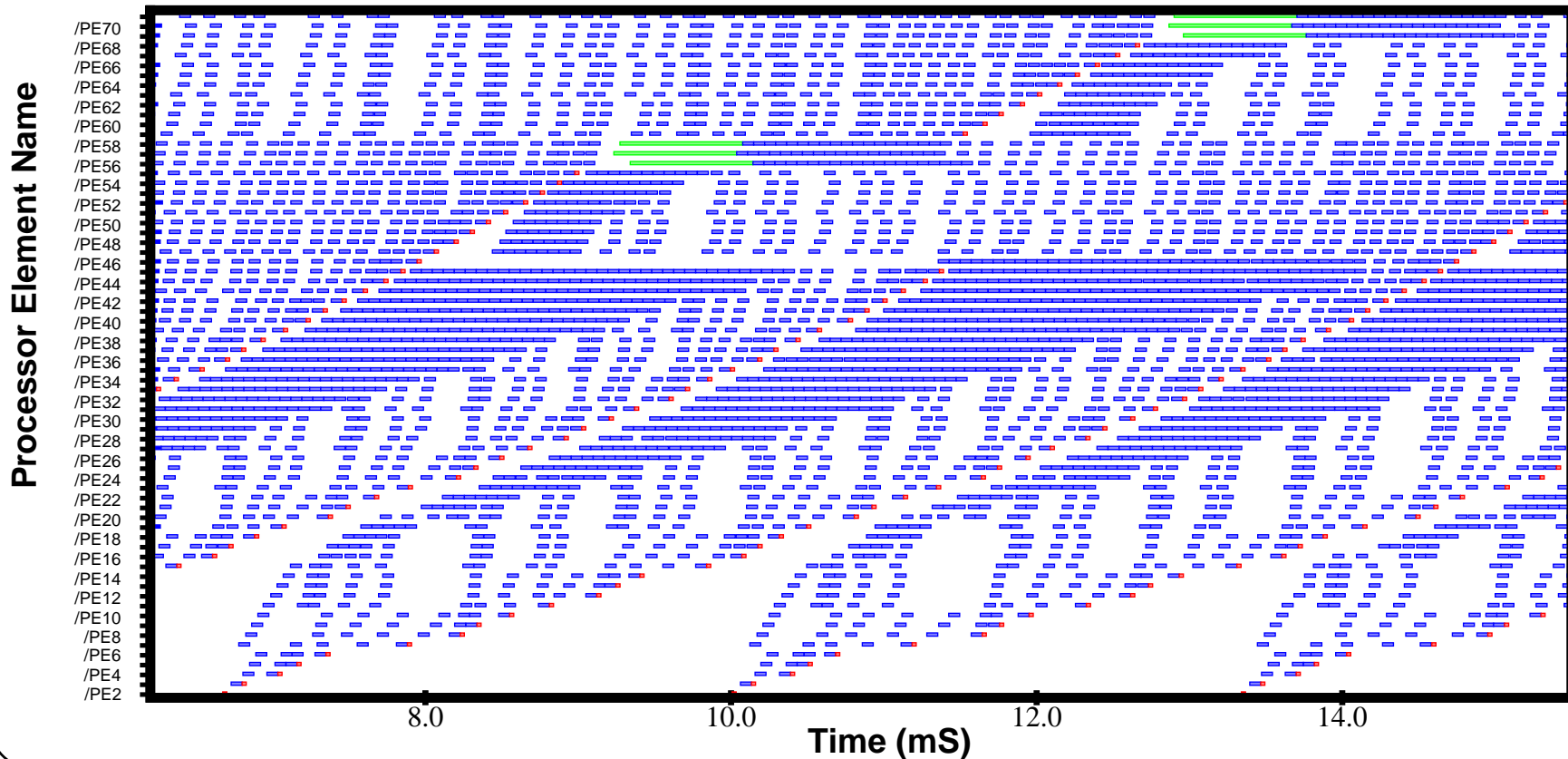


## Time-Line: Block-Recursive RMGS Algorithm Mapped to HPSC/Myrinet Architecture



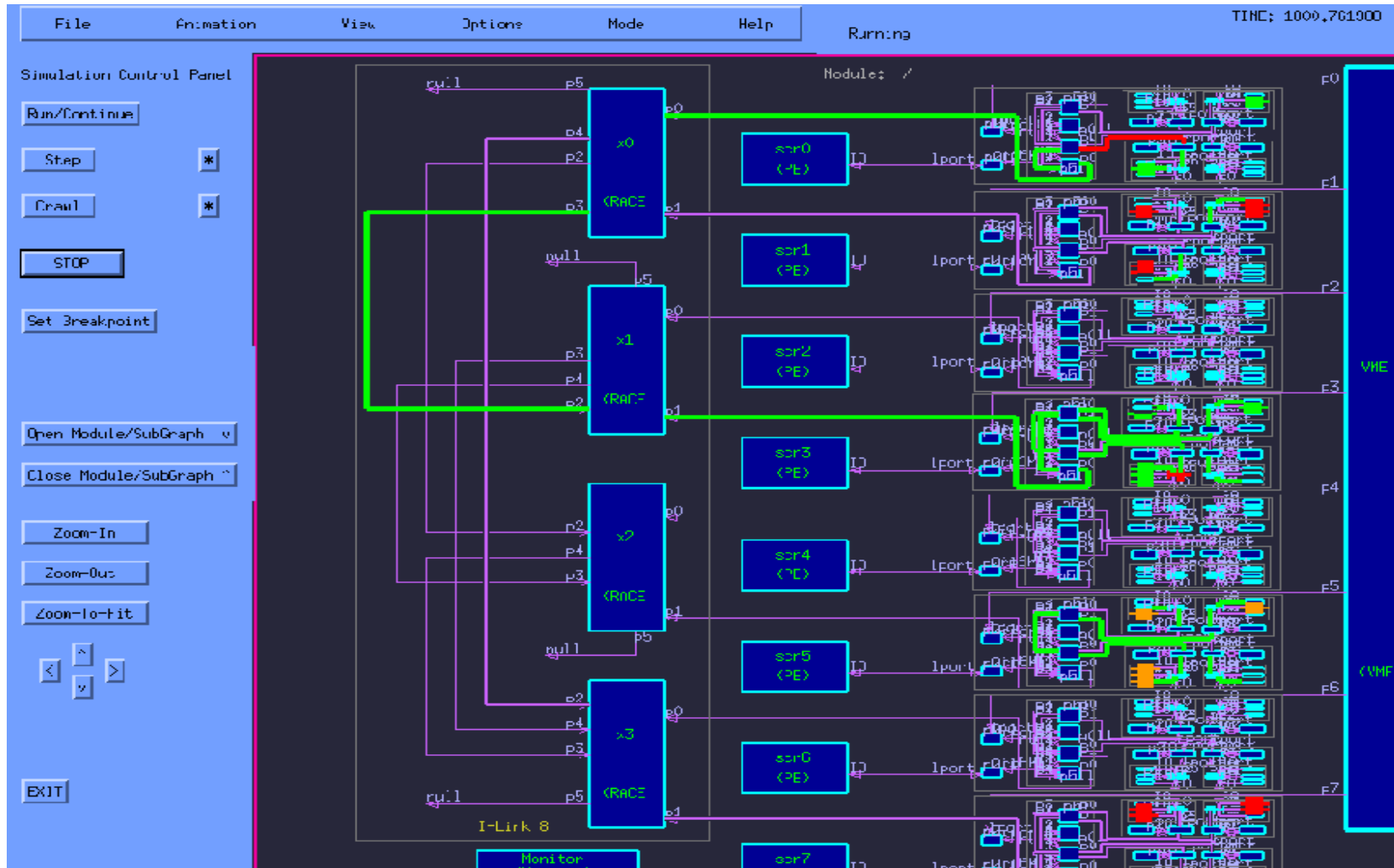
## Virtual Prototype Example

- Previous time-line assumed data transfer overhead = 40-cycles (1-uS)
- Initial estimate proved optimistic. First hardware measured much higher.
- Effect of overhead size was easily examined with performance model.
- Below is same graph, but assuming 200-cycle (5-uS) transfer overhead.
- Note severe skew & poor utilization in aggregate due to comm.-overhead.



# Demo Test for DSP System Virtual Prototype

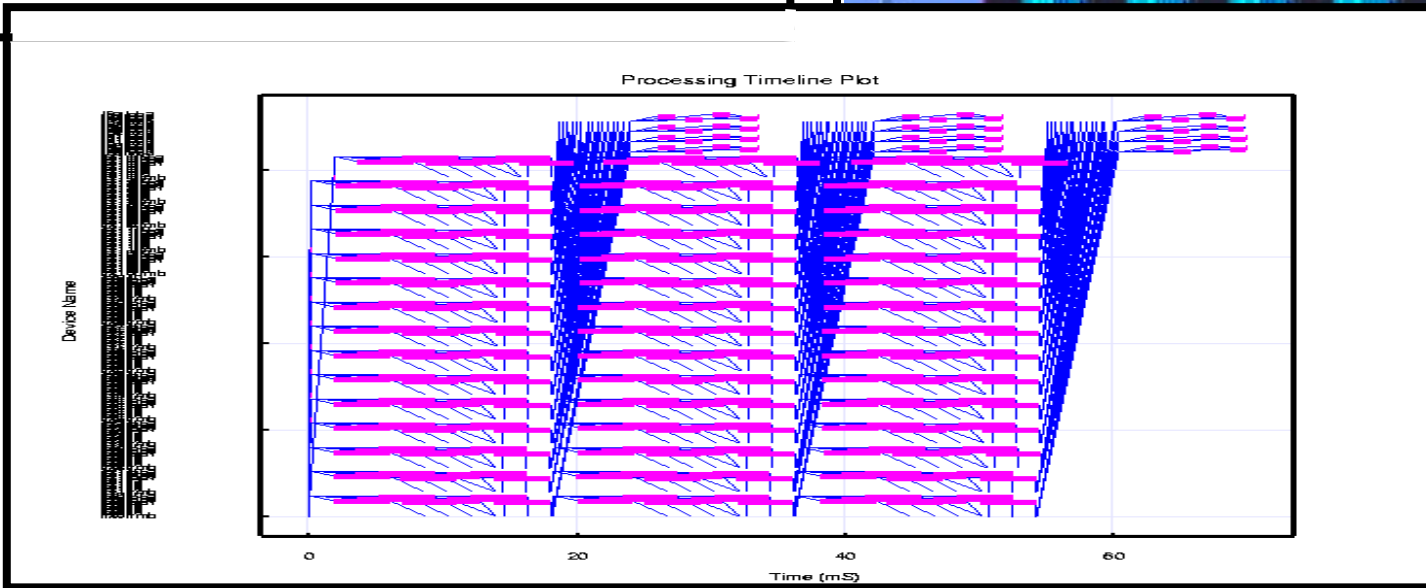
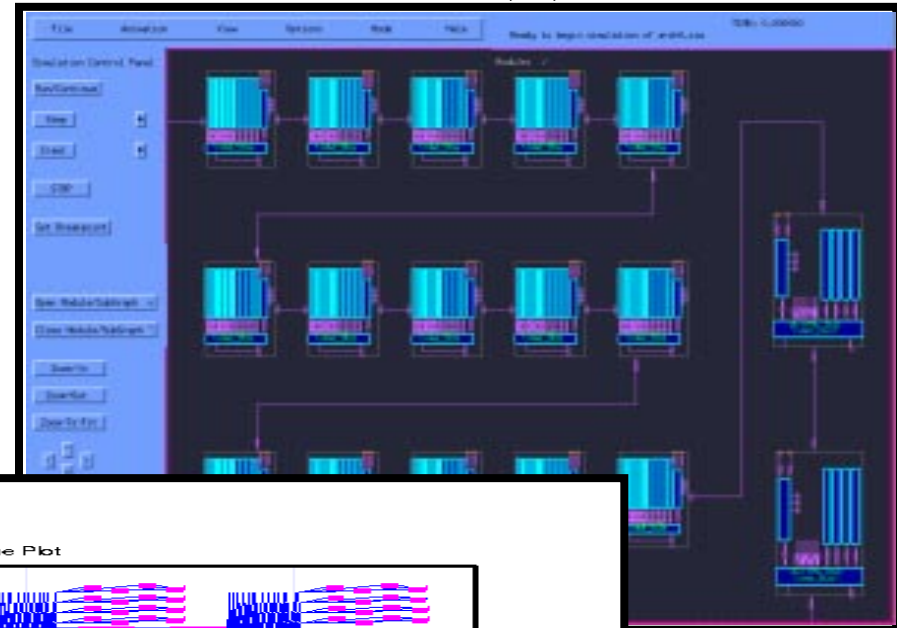
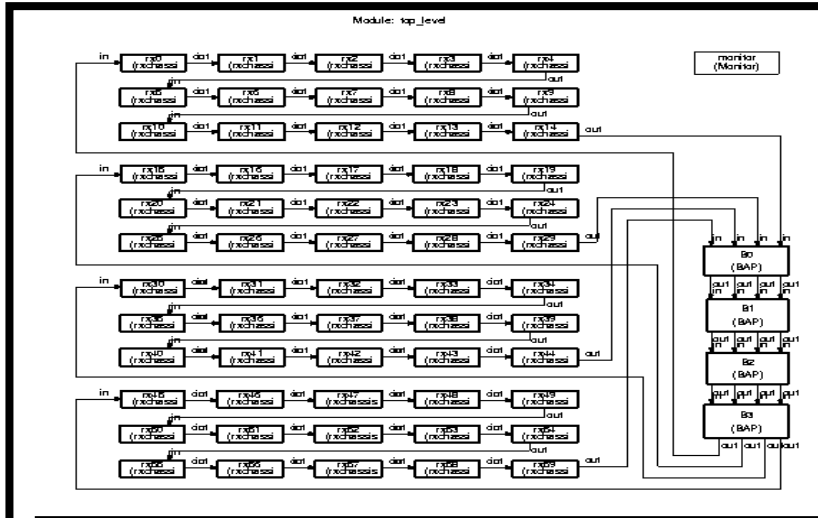
- Snapshot of 400+ Processor Animation
- Mercury Raceway network based.



# Radar System

## Digital Pulse Compression and Beamformer

> 60 VME Chassis, 1,000+ Processors



## Summary

- **Role of Virtual-Prototypes.**
  - Hardware / Software design, optimization.
  - Task scheduling / mapping.
  - Network architecture evaluation.
- **Virtual-Prototypes Offer:**
  - Non-invasive observability, unequaled by physical prototypes.
  - Available early in design process. Less costly than physical prototyping.
  - More rapid design evolution. (Make and evaluate changes in seconds.)
  - Special techniques and tools needed for efficiency and accuracy.
- **For more examples and information, see:**

[www.atl.lmco.com/proj/csim](http://www.atl.lmco.com/proj/csim)

(Full Documentation on-line.)

